DETAILED ACTION

Response to Amendment

1. Claims 1-8 were formerly rejected under 35 U.S.C. 103 (a). Pursuant to applicant's amendments these rejections have been withdrawn.

2. Claims 1-8 were formerly rejected under 35 U.S.C. 112 second paragraph. Pursuant to applicant's amendments these rejections have been withdrawn.

Response to Arguments

3. Applicant's arguments, see Remarks filed July 15, 2011 with respect to claims 1-7 have been fully considered and are persuasive. The 35 U.S.C. 103 (a) rejections of claims 1-8 have been withdrawn. Applicant argues Hoeniger is a ring and does not have a bus end. Examiner respectfully disagrees with the applicant. There is no mention of "ring" in the Hoeniger reference. The bus architecture of Hoeniger is serial (figure 2, column 7, lines 47-67, wherein the last node 400n is considered the bus end since it is furthest away from the host). The loop back feature (405) that is shown is only for control purposes of the shift register (column 8, 10-15) and thus does not make the bus a ring.

Claim Rejections - 35 USC § 103

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoenniger, III et al. (US 4,885538, hereinafter Hoenniger) in view of Machida et al.(US 6,122,257, hereinafter Machida).

Regarding **claim 1**, Hoenniger discloses a system for transmitting data in bi-directional bus with at control device comprising a send and receiving unit for data fields combined into a data frame(column 10, lines 1-27, figure 2, wherein 100 is the control device) and with bus subscribers (figure 2) with at least the bus subscriber at the bus end opposite of the control device comprising a send device for a data frame (figure 2, each subscriber is able to

transmit)wherein at least the bus subscriber at the end of the bus comprises a control stage which is activated by a received frame sent by a control device over the serial bi-directional bus and triggers the send device depending on the receipt of a data frame within the terms of the transmission of a data frame for at least the data fields of the bus subscribers(column 10, lines 45-67, column 11, lines 21-45) for sending a data frame over the serial bidirectional bus in the direction of the control device (1) (column 11, lines 65-67, column 12, lines 1-12) whereas the sent data frame contains at least data fields (14,15,16) for all bus subscribers and the data frame is handed over from one bus subscriber to the next bus subscriber (column 11, lines 49-67). Hoenniger does not disclose wherein each bus subscriber comprises a test circuit to determine whether it is located at the bus end opposite of the control device. Goodman discloses wherein each bus subscriber comprises a test circuit to determine whether it is located at the bus end opposite of the control device (¶[0049]-¶[0051], wherein the processor nodes (subscribers) include relative location and test circuits ,¶[0058] , the processor at the end of the bus will only have one adjacent processor node). Thus, it would have been obvious to the one of ordinary skill in the art at the time of invention to utilize the teachings as disclosed by Goodman along with the system of Hoenniger .The test circuit as disclosed by Machida can be implemented in the system of Hoenniger through hardware implementation. The motivation for utilizing the test circuit as disclosed by Goodman along with the system of Hoenniger is to increase the efficiency of the system by detecting and isolating errors by determining the location and position of each subscriber(Goodman, ¶[0050]).

Regarding **claim 2** Hoenniger discloses wherein each of the bus subscribers comprises a control stage for a send device for sending a data frame for the own data fields and the data fields

of the bus subscribers which lie between the control device and the respective bus subscribers (column 10, lines 45-50)

Regarding **claim 3**, Hoenniger discloses the bus subscribers comprise a memory for the position of the data fields within the respective data frame which data fields can be read in and out via the evaluation circuit (¶[[0028],¶[[0025]).

Regarding **claim 4**, Hoenniger discloses the control device comprises an allocation stage for the position of the data fields within a data frame which can be allocated to the individual bus subscribers (figure 2A, wherein 192,194..are the data fields, column 10, lines 60-67) and an initialization device for reading out the positional data in data fields of a data frame addressed to the individual bus subscribers(column 11, lines 20-45), and that the bus subscribers comprise an initialization circuit for the address-related reading out of the positional data from the addressed data fields of the data frame into the memory for these positional data(column 15, lines 1-30, column 15, lines 60-67).

Regarding **claim 5**, Hoenniger discloses each bus subscriber comprises a test circuit for recognizing a bus subscriber connected to the bus and connected in outgoing circuit with the same (column 15, lines 50-67, column 14, lines 35-50, figure 3A).

Regarding **claim 6**, Hoennigerr discloses the control device and the bus subscribers each comprise an encoding device for producing check data from the data frame and that, as is known, the control device and the bus subscribers each comprise a check device for check data received with the data frames(column 15, lines 1-10).

Regarding **claim 7**, Hoennigerr discloses the control device comprises an address memory for the addresses of the bus subscribers(column 5, lines 38-52, column 7, lines 65-67-

column 8, lines 1-5) and that each bus subscriber comprises a recognition circuit for triggering the evaluation circuit for reading out the data field in the data frame addressed to the bus subscriber on the one hand and for reading in its data field into the data frame on the other hand (column 15, lines 50-67, column 14, lines 35-50, figure 3A)

Regarding **claim 8,** Hoenniger discloses multiple data fields are sent simultaneously in a single data frame at a time (figure 2A).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANGEL BROCKMAN whose telephone number is (571)270-5664. The examiner can normally be reached on Monday-Friday ,7:30-5:00pm.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derrick Ferris can be reached on 571-272-3123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANGEL BROCKMAN

Examiner
Art Unit 2463

/A. B./
Examiner, Art Unit 2463

/Derrick W Ferris/

Supervisory Patent Examiner, Art Unit 2463